Memorandum of Understanding
Centre of Excellence on VLSI and Embedded System
Hands-on Skill Development Program on Semiconductor Technologies
In-Campus Establishment of Centre of Excellence of VLSI & Embedded System in BBDITM in collaboration with PinE Training Academy (Training Division of Aujas Technology, Noida)

This Memorandum of Understanding is signed on the 15th November, 2021 between the following institutions:

A. Mr. Vaibhav Mishra – Founder of PinE training academy (Training division of Aujas Technology Private Limited) referred as PTALLP, C56/36,1st Floor Sector 62, Noida, UP, 201301, India
B. Dr. Shailendra Singh Chauhan – Director of BBDITM, Ayodhya Road, Lucknow 226028, (referred to as BBDITM hereafter).

This MoU is proposed to develop the foundation of the semiconductor technologies like ASIC Design & Full Custom Layout, DFT, Physical Design, FPGA, Embedded, PCB and ASIC Verification for ECE students of BBDITM by PinE Training Academy LLP referred to as PTALLP – a training division of Aujas Technology. Through this Memorandum of Understanding, the two parties agree to the following:

Scope of the MoU (General Terms):

1. PTALLP will run a core electronics skill development on ET in accordance with the technical content (Attached in Annexure-I) from July 2022 – July 2023 (for the 1-year academic session) during weekends/weekdays or on public holidays after or before college hours/on-line mode.
2. The course will be run for up to a minimum of 5 and maximum of 30 students per batch for each ET.
3. 2nd and 3rd year hands-on core electronics learning in BBDITM Campus and training of 4th year will run in PTALLP campus (optional), learning content is attached for 2nd, 3rd and 4th year in all ET (ASIC Design & Full Custom layout , DFT , Physical Design , FPGA, Embedded, PCB and ASIC Verification referred to as ET).
4. BBDITM will allow a minimum of [illegible] for interaction session with the 2nd to 4th year in every semester and with the 1st year in the 1st and 2nd semester before any technical learning plan. During this interactive session, PTALLP will plan hands-on orientation on Hardware Digital Design and feature domains like Analog and RFL.
5. There is no financial commitment on the part of BBDITM.

Commitments from the PTALLP side:

1. Trainer/Mentor from PTALLP will conduct the technical learning on weekends or weekdays or on Public holidays/Leaves.
2. Other than the interaction session, the learning session will be a minimum of 2hrs for each batch depending on the BBDITM technical course (with adequate breaks in between – at least one 15 minutes break).
3. PTALLP will run the course with min 5 students at the BBDITM campus.
4. After placement through PTALLP as an internship or full-time employee, the trainee's offer letter will share with the college ECE department and the College Training Placement cell.
5. PTALLP will work closely with the ECE Department and Placement cell to place trainees in Core Electronics.
6. PTALLP will share the training calendar in advance as well as the registration of students to the ECE department.

Commitment from BBDITM side:

1. BBDITM will provide the necessary infrastructure to set up CoE Lab as follows: desktop (Computers), one training room, and a room equipped with chairs and tables, projector, power supply, etc.
2. BBDITM will allow PTALLP to interact with students from 2nd year to 4th onwards through the demo, workshop, and tax sessions to get students for registration in CoE.

Validity of the MoU

1. MoU validity as per the academic calendar. In case of termination, both parties PTALLP and BBDITM will bring in notice one month before and will consider one month's notice period before discontinuing.

Authorized Signatories: **Authorized Signatory**

PinE Training Academy: **BBDITM, Lucknow**

Director
BBDITM, Lucknow